

Contents

1	Introduction	8
1.1.	General Remarks	8
1.2.	Contents of this Documentation	8
1.3.	Naming Conventions	8
1.4.	Additional Products and Documents	8
1.4.1.	Hardware Products	8
1.4.2.	Software Products	9
1.5.	Documents and References	9
1.5.1.	Syslogic Documentation	9
1.5.2.	Standards and Books	9
1.5.3.	Datasheets	9
1.6.	Items delivered	10
1.7.	Safety Recommendations and Warnings	10
1.8.	Electro-Static Discharge	10
1.9.	Life Cycle Information	10
1.9.1.	Transportation and Storage	10
1.9.2.	Operation	10
1.9.3.	Maintenance and Repair	11
1.9.4.	Warranty	11
1.9.5.	RoHS	11
1.9.6.	Disposal and WEEE	11
2	Product Description	12
2.1.	IPC/COMPACT7-SL Systems	12
2.2.	Features of the IPC/COMPACT7L5-1A	12
2.2.1.	CPU Core	12
2.2.2.	Memory	12
2.2.3.	Graphics Controller	12
2.2.4.	CompactFlash and IDE Interface (Parallel ATA)	13
2.2.5.	Integrated Peripherals	13
2.2.6.	PS/2 Mouse and Keyboard Interface	13
2.2.7.	Serial Ports	13
2.2.8.	Universal Serial Bus	13
2.2.9.	Ethernet	13
2.2.10.	Firmware Flash Memory	14
2.2.11.	Real Time Clock	14
2.2.12.	Configuration Switches	14
2.2.13.	Power Supply	14
2.3.	Features of the IPC/COMPACT7L1-1A	14
2.3.1.	CPU Core	14
2.3.2.	Memory	14
2.3.3.	Graphics Controller	15

2.3.4.	CompactFlash and IDE Interface (Parellel ATA)	15
2.3.5.	Integrated Peripherals	15
2.3.6.	PS/2 Mouse and Keyboard Interface	15
2.3.7.	Serial Ports	16
2.3.8.	Universal Serial Bus	16
2.3.9.	Ethernet	16
2.3.10.	Firmware Flash Memory	16
2.3.11.	Real Time Clock	16
2.3.12.	Configuration Switches	16
2.3.13.	Power Supply	16
2.4.	Features of the IPC/COMPACT7M1-1A	16
2.4.1.	CPU Core	16
2.4.2.	Memory	17
2.4.3.	Graphics Controller	17
2.4.4.	CompactFlash and IDE Interface (Parellel ATA)	17
2.4.5.	Integrated Peripherals	18
2.4.6.	PS/2 Mouse and Keyboard Interface	18
2.4.7.	Serial Ports	18
2.4.8.	Universal Serial Bus	18
2.4.9.	Ethernet	18
2.4.10.	Firmware Flash Memory	18
2.4.11.	Real Time Clock	18
2.4.12.	Configuration Switches	18
2.4.13.	Power Supply	18
3	Hardware Description	20
3.1.	Overview	20
3.2.	Memory and I/O Resources	22
3.2.1.	General Memory Layout and Configuration	22
3.2.2.	General I/O Layout and Configuration	24
3.3.	Intel Atom Z5xx Processor	26
3.4.	Intel System Controller Hub US15W	26
3.5.	PCI/PCIe Devices	27
3.6.	Hardware Interrupts	28
3.7.	DMA Channels	28
3.8.	Peripheral Devices	29
3.8.1.	Scope	29
3.8.2.	DVI Interface	29
3.8.3.	LVDS Interface	31
3.8.4.	VGA Interface	32
3.8.5.	IDE/CompactFlash-Interface	33
3.8.6.	Serial Ports 1/2	35
3.8.7.	USB Interface	35
3.8.8.	PS/2 Keyboard/Mouse Interface	36
3.8.9.	Ethernet Interfaces	37

3.8.10.	Watchdog	38
3.8.11.	Power Supervision	38
3.8.12.	Configurations Switches	39
3.8.13.	Factory Programming Header	39
3.8.14.	LPC Header	39
3.8.15.	Isolated Power Supply	39
3.9.	Optional Functions	40
3.10.	Hardware Limitations	40
4	Programming Information	41
4.1.	Overview	41
4.2.	Interrupt, Memory and I/O Resources	41
4.2.1.	Interrupt Resources	41
4.2.2.	Memory Resources	41
4.2.3.	I/O Resources	41
4.3.	Peripheral Devices	47
4.3.1.	VGA-Interface	47
4.3.2.	IDE-Interface	47
4.3.3.	Serial Ports	47
4.3.4.	Keyboard/Mouse Interface	47
4.3.5.	Ethernet Interfaces	47
4.3.6.	Temperature Sensor	47
4.3.7.	Watchdog	48
5	Enclosure, Assembly and Mounting	49
5.1.	IPC/COMPACT7-SL Dimensions	49
5.2.	Internal Cabling	49
5.3.	Serviceable Parts	49
5.4.	Final Mounting of the Enclosure	52
5.4.1.	Rear Mounting	52
5.4.2.	Vertical Bottom Mounting	53
5.4.3.	Horizontal Bottom mounting	54
5.4.4.	DIN Rail Mounting	55
6	Installation and Cabling	56
6.1.	Introduction	56
6.2.	Powering the IPC/COMPACT7-SL System	56
6.3.	Cabling the Interfaces	57
6.4.	Grounding	58
6.5.	Cabling of Communication Links	59
7	Technical Data	61
7.1.	Electrical Data	61
7.2.	EMI / EMC Specification	64
7.2.1.	Relevant Standards	64

7.2.2.	Emission	64
7.2.3.	Immunity	65
7.3.	Environmental Specification	65
7.4.	Mechanical Data	66
8	Firmware	67
8.1.	Software Structure	67
8.2.	Application Programming Interface (API)	67
8.3.	Operating Systems	68
9	Product Revision History	69
9.1.	Hardware	69
9.2.	Firmware/BIOS	69
10	Manufacturer Information	70
10.1.	Contact	70

List of Tables

Tab. 1	Physical Memory Address Space Layout for IPC/COMPACT7M1-1A	22
Tab. 2	I/O Address Space Layout	25
Tab. 4	PCI Devices	27
Tab. 5	Hardware Interrupt Table	28
Tab. 6	DMA channels	28
Tab. 7	DVI-D connector P5	30
Tab. 8	LVDS header P3	32
Tab. 9	VGA header J1	32
Tab. 10	IDE Configuration Options	33
Tab. 11	IDE Connector P7 (2x22 pin)	34
Tab. 12	Serial Ports COM1 and COM2	35
Tab. 13	Keyboard/Mouse Configuration Options	36
Tab. 14	Keyboard/Mouse internal Header J6 (2x5 pin)	37
Tab. 15	Ethernet Twisted Pair Interface Connector P18 and P19 (RJ45)	37
Tab. 16	Watchdog Configuration Options	38
Tab. 17	Factory Programming Header J5 (2x5 pin)	39
Tab. 18	LPC J3 (1x7 pin)	39
Tab. 19	IPC/NETSBC-7A System Registers	41
Tab. 20	I2C Address Space	47
Tab. 21	Power connector pinout	56
Tab. 22	Weidmüller power connector	57
Tab. 23	IPC/COMPACT7M71-1A: Connectors	58
Tab. 24	General Absolute Maximum Ratings	61
Tab. 25	General Recommended Operating Conditions	62
Tab. 26	General Electrical Characteristics	62
Tab. 27	General Switching Characteristics	63
Tab. 28	Electromagnetic Emission	64
Tab. 29	Electromagnetic Immunity	65
Tab. 30	Hardware Revision State	69
Tab. 31	BIOS Revision State	69

List of Figures

Fig. 1	Block Diagram (IPC/NETSBC-7A)	19
Fig. 2	Board Layout (IPC/NETSBC-7X).....	21
Fig. 3	Memory Map	23
Fig. 4	Intel Atom Processor Z5xx	26
Fig. 5	Intel System Controller Hub US15W	26
Fig. 6	PCI Express System	27
Fig. 7	Watchdog Blockdiagram	48
Fig. 8	IPC/COMPACT7M1-1A.....	49
Fig. 9	Service of battery or Compact Flash card.....	51
Fig. 10	Rear mounting of the IPC/COMPACT7-SL (product image may vary).....	52
Fig. 11	Vertical bottom mounting of the IPC/COMPACT7-SL (product image may vary) ..	53
Fig. 12	Horizontal bottom mounting of the IPC/COMPACT7-SL (product image may vary) 54	
Fig. 13	One possible way of mounting the IPC/COMPACT6-SL onto the DIN-Rail.....	55
Fig. 14	Front view with connector markings (product image may vary).....	57
Fig. 15	Additional grounding of the cable shields at the entry point of a cabinet.	59
Fig. 16	Non isolated communication link with common chassis potential.....	60
Fig. 17	Isolated communication link.....	60

1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.

Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.

Syslogic is grateful for any help referring to errors or for suggestions for improvements.

The following registered trademarks are used:

IBM-PC, PC/AT, PS/2	trademarks of IBM Corporation
i ² C	trademark of Philips Corporation
CompactFlash	trademark of SanDisk Corporation
PC/104	trademark of PC/104 Consortium
PCI/104	trademark of PC/104 Consortium
Intel Atom	trademark of Intel Corporation
Windows Embedded Compact	trademark of Microsoft Corporation
Windows Embedded Standard	trademark of Microsoft Corporation

All other trademarks appearing in this document are the property of their respective company.

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the system. It provides all information needed to configure, setup and program the IPC/COMPACT7xx-1A system.

1.3. Naming Conventions

The exact product identifications are IPC/COMPACT7L5-1A, IPC/COMPACT7L1-1A and IPC/COMPACT7M1-1A. Throughout this documentation the product is reference through it's marketing name "IPC/COMPACT7-SL".

The same applies to the integrated base board. The exact board identification is IPC/NETSBC-7A. Throughout this documentation it will be referenced as "NETSBC-7A".

1.4. Additional Products and Documents

1.4.1. Hardware Products

In order to mount the IPC/COMPACT7-SL correctly there are four different mounting kits which have to be ordered separately:

- IPC/MKITCP-1A: for rear mounting (DOC/IPC_MKITCP-1AE)
- IPC/MKITCP-2A: for bottom mounting (DOC/IPC_MKITCP-2AE)
- IPC/MKITCP-2C: for bottom mounting (DOC/IPC_MKITCP-2CE)
- IPC/MKITCP-2E: DIN rail kit (DOC/IPC_MKITCP-2EE)

For further assistance and information please contact the manufacturer.

1.4.2. Software Products

There are no additional software products except operating systems:

- Operating Systems: check chapter 6.4 for a list of supported implementations.

1.5. Documents and References

1.5.1. Syslogic Documentation

The following documents are *required* for correct installation and operation of the IPC/COMPACT6-SL:

- DOC/IPC_MKITCP-1AE: information on rear mounting
- DOC/IPC_MKITCP-2AE: information on bottom mounting
- DOC/IPC_MKITCP-2CE: information on bottom mounting
- DOC/IPC_MKITCP-2EE: information on DIN rail mounting

1.5.2. Standards and Books

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- PCI/104 Specification Version 1.0
- IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
- IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
www.ieee.org
- 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego), ISBN 0-929392-15-9
- 'PCI System Architecture' by Tom Shanley / Don Anderson (Mindshare, Inc.), ISBN 0-201-30974-2

1.5.3. Datasheets

For additional and more detailed information on the Intel Atom processor and chipset the following documents are of interest:

- Datasheet Intel Atom Processor Z5xx Series
<http://download.intel.com/design/processor/datashts/319535.pdf>
- Specification Update Intel Atom Processor Z5xx Series
<http://download.intel.com/design/processor/specupdt/319536.pdf>

- Datasheet Intel System Controller Hub (SCH)
<http://download.intel.com/design/chipsets/embedded/datashts/319537.pdf>
- Specification Update Intel System Controller Hub (SCH)
<http://download.intel.com/design/chipsets/embedded/specupdt/319538.pdf>
- Datasheet Addendum Intel System Controller Hub (SCH)
<http://download.intel.com/design/chipsets/embedded/datashts/321422.pdf>
- Datasheet Intel 82574 GbE Controller Family
<http://download.intel.com/design/network/datashts/82574.pdf>

1.6. Items delivered

- The IPC/COMPACT7-SL comes with an IPC/NETSBC-7A base board and an enclosure. Mounting kits have to be ordered separately.

1.7. Safety Recommendations and Warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.

The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.

The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.

In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 10). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

1.8. Electro-Static Discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in a ESD protected environment. Otherwise a proper operation is not guaranteed and the warranty is not applicable.

1.9. Life Cycle Information

1.9.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains a box with antistatic and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.9.2. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.

The main functionality of the IPC system is defined by the application programs running on the processor board. The operating system and application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.9.3. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (ESD and mechanical protection).

1.9.4. Warranty

Our products are covered by a world-wide manufacturers warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a serial number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.

The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged or operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

1.9.5. RoHS

The products of the IPC/COMPACT7-SL family are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC).

1.9.6. Disposal and WEEE

At the end of the life span the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.

The products of the IPC/COMPACT7-SL are not designed ready for operation for the end-user and intended for consumer applications. Therefore the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable. But users should still dispose the product properly at the end of life.

2 Product Description

2.1. IPC/COMPACT7-SL Systems

The IPC/COMPACT7-SL contains an enclosure and the IPC/NETSBC-7A motherboard. A list of main features of the motherboard can be found below:

2.2. Features of the IPC/COMPACT7L5-1A

2.2.1. CPU Core

- **Intel Atom Z510** (Silverthorne) single core processor for mobile devices
- IA32 processor based on Intel's 45nm Hi-k metal gate silicon technology
- Multiple micro-ops per instruction are combined into one micro-op and executed in a single cycle
- In-order execution core
- high performance 32-bit 16-stage pipeline
- energy efficient branch prediction
- 400MHz front side bus supporting CMOS levels on address and data lines
- FSB with 64bit data width and 32bit address bus
- 64bit data width, 32bit address bus
- **1.1GHz processor clock**
- 32kB instruction and 24kB data L1 cache
- Dynamic L2 cache sizing: max. 512kB
- 64-bit wide DDR SDRAM interface
- enhanced Intel Speedstep Technology

2.2.2. Memory

- **512 Mbyte DDR2 SDRAM** on board (device width x16)
- 400MT/s data rate
- 64bit data width

2.2.3. Graphics Controller

- integrated Intel Graphics Media Accelerator 500 (Intel GMA500)
- integrated graphics device (IGD) includes LVDS and SDVO display ports
- max pixel clock 112MHz (equates to 1376x768 @ 85Hz)
- SDVO max. pixel clock 160MHz (equates to 128x1024 @ 85Hz)
- Supports Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3)
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9
- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards

- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

2.2.4. CompactFlash and IDE Interface (Parallel ATA)

- 1 port supporting 2 devices (master/slave)
- PIO modes 0, 1, 2, 3, 4
- Single word DMA modes 0, 1, 2
- Multi-word DMA modes 0, 1, 2
- Ultra-DMA modes 0, 1, 2, 3, 4, 5
- Up to 100 Mbytes/s in UDMA-100 mode
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

2.2.5. Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

2.2.6. PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- Only available on an internal header

2.2.7. Serial Ports

- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit FIFO (16550)

2.2.8. Universal Serial Bus

- Four USB V2.0 ports (OHCI/EHCI-Host Controller)

2.2.9. Ethernet

- Two 10/100/1000 baseT Ethernet interfaces

2.2.10. Firmware Flash Memory

- 8 MBit BootBlock Flash for BIOS and setup data (excluding date and time)

2.2.11. Real Time Clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through onboard battery or header

2.2.12. Configuration Switches

- Two rotary hex switches for customer application

2.2.13. Power Supply

- Onboard non-isolated power supply with wide input range (10Vdc ... 30Vdc)
- Configurable power supply supervision (this function is only available on systems with revision 3 or higher)
- Monitors either external power supply voltage or it can be used as external power fail or on/off input (this function is only available on systems with revision 3 or higher)
- Optional isolated power supply

2.3. Features of the IPC/COMPACT7L1-1A

2.3.1. CPU Core

- **Intel Atom Z510** (Silverthorne) single core processor for mobile devices
- IA32 processor based on Intel's 45nm Hi-k metal gate silicon technology
- Multiple micro-ops per instruction are combined into one micro-op and executed in a single cycle
- In-order execution core
- high performance 32-bit 16-stage pipeline
- energy efficient branch prediction
- 400MHz front side bus supporting CMOS levels on address and data lines
- FSB with 64bit data width and 32bit address bus
- **1.1GHz processor clock**
- 32kB instruction and 24kB data L1 cache
- Dynamic L2 cache sizing: max. 512kB
- 64-bit wide DDR SDRAM interface
- enhanced Intel Speedstep Technology

2.3.2. Memory

- **1024 Mbyte DDR2 SDRAM** on board (device width x16)
- 400MT/s data rate

- 64bit data width

2.3.3. Graphics Controller

- integrated Intel Graphics Media Accelerator 500 (Intel GMA500)
- integrated graphics device (IGD) includes LVDS and SDVO display ports
- max pixel clock 112MHz (equates to 1376x768 @ 85Hz)
- SDVO max. pixel clock 160MHz (equates to 128x1024 @ 85Hz)
- Supports Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3)
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9
- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

2.3.4. CompactFlash and IDE Interface (Parallel ATA)

- 1 port supporting 2 devices (master/slave)
- PIO modes 0, 1, 2, 3, 4
- Single word DMA modes 0, 1, 2
- Multi-word DMA modes 0, 1, 2
- Ultra-DMA modes 0, 1, 2, 3, 4, 5
- Up to 100 Mbytes/s in UDMA-100 mode
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

2.3.5. Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

2.3.6. PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- Only available on an internal header

2.3.7. Serial Ports

- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit FIFO (16550)

2.3.8. Universal Serial Bus

- Four USB V2.0 ports (OHCI/EHCI-Host Controller)

2.3.9. Ethernet

- Two 10/100/1000 baseT Ethernet interfaces

2.3.10. Firmware Flash Memory

- 8 MBit BootBlock Flash for BIOS and setup data (excluding date and time)

2.3.11. Real Time Clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through onboard battery or header

2.3.12. Configuration Switches

- Two rotary hex switches for customer application

2.3.13. Power Supply

- Onboard non-isolated power supply with wide input range (10Vdc ... 30Vdc)
- Configurable power supply supervision (this function is only available on systems with revision 3 or higher)
- Monitors either external power supply voltage or it can be used as external power fail or on/off input (this function is only available on systems with revision 3 or higher)
- Optional isolated power supply

2.4. Features of the IPC/COMPACT7M1-1A

2.4.1. CPU Core

- **Intel Atom Z530** (Silverthorne) single core processor for mobile devices
- IA32 processor based on Intel's 45nm Hi-k metal gate silicon technology
- Multiple micro-ops per instruction are combined into one micro-op and executed in a single cycle
- In-order execution core

- high performance 32-bit 16-stage pipeline
- energy efficient branch prediction
- 533MHz front side bus supporting CMOS levels on address and data lines
- FSB with 64bit data width and 32bit address bus
- **1.6GHz processor clock**
- 32kB instruction and 24kB data L1 cache
- Dynamic L2 cache sizing: max. 512kB
- 64-bit wide DDR SDRAM interface
- supports Intel Hyper Threading Technology (HTT), 2 threads
- supports Intel Virtualization Technology (VT-x)
- enhanced Intel Speedstep Technology

2.4.2. Memory

- **1024 Mbyte DDR2 SDRAM** on board (device width x16)
- 533MT/s data rate
- 64bit data width

2.4.3. Graphics Controller

- integrated Intel Graphics Media Accelerator 500 (Intel GMA500)
- integrated graphics device (IGD) includes LVDS and SDVO display ports
- max pixel clock 112MHz (equates to 1376x768 @ 85Hz)
- SDVO max. pixel clock 160MHz (equates to 128x1024 @ 85Hz)
- Supports Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3)
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9
- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

2.4.4. CompactFlash and IDE Interface (Parallel ATA)

- 1 port supporting 2 devices (master/slave)
- PIO modes 0, 1, 2, 3, 4
- Single word DMA modes 0, 1, 2
- Multi-word DMA modes 0, 1, 2
- Ultra-DMA modes 0, 1, 2, 3, 4, 5
- Up to 100 Mbytes/s in UDMA-100 mode
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

2.4.5. Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

2.4.6. PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- Only available on an internal header

2.4.7. Serial Ports

- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit FIFO (16550)

2.4.8. Universal Serial Bus

- Four USB V2.0 ports (OHCI/EHCI-Host Controller)

2.4.9. Ethernet

- Two 10/100/1000 baseT Ethernet interfaces

2.4.10. Firmware Flash Memory

- 8 MBit BootBlock Flash for BIOS and setup data (excluding date and time)

2.4.11. Real Time Clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through onboard battery or header

2.4.12. Configuration Switches

- Two rotary hex switches for customer application

2.4.13. Power Supply

- Onboard non-isolated power supply with wide input range (10Vdc ... 30Vdc)
- Optional isolated power supply

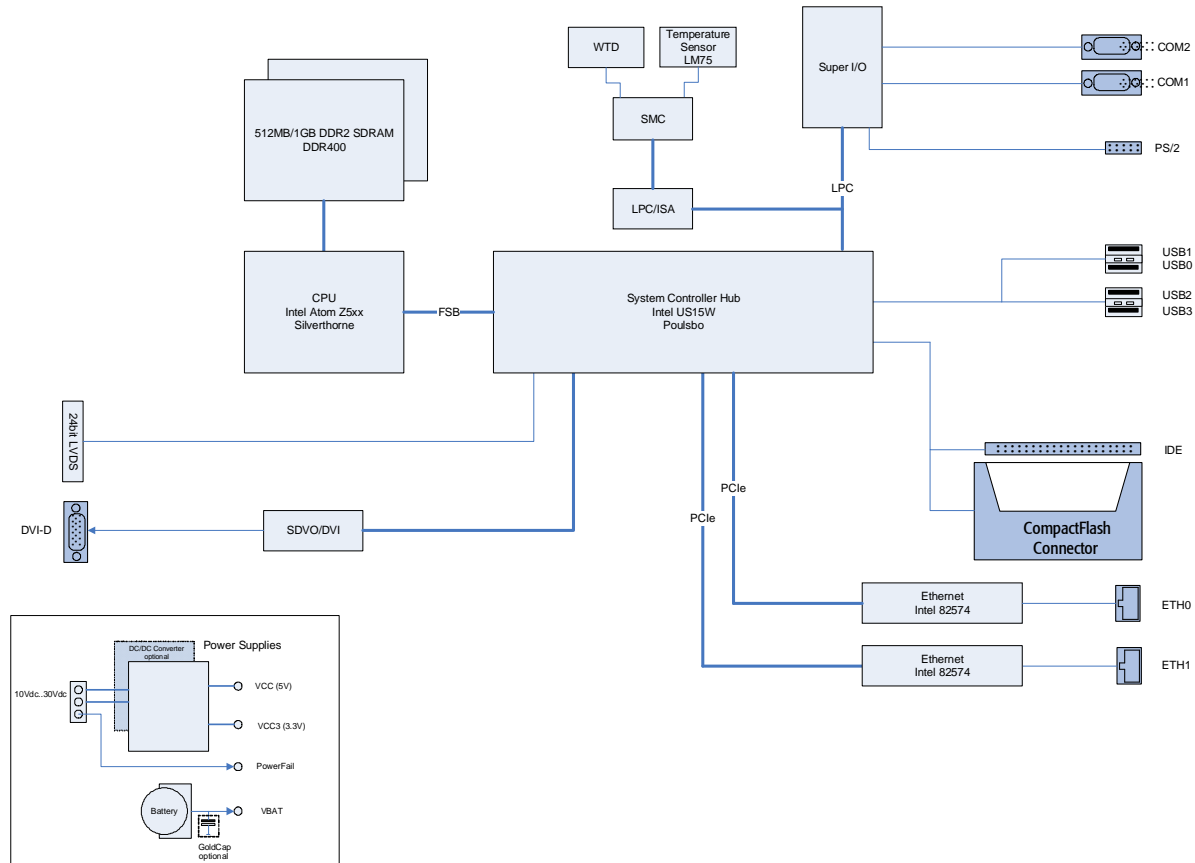


Fig. 1 Block Diagram (IPC/NETSBC-7A)

3 Hardware Description

3.1. Overview

The IPC/NETSBC-7A board hardware may be configured by software (BIOS) and by jumper setting. Software configuration should always be done by using the BIOS Setup. The BIOS Setup can be entered by pressing <F2> or at power-up.

The jumper and connector locations are shown in the board layout drawing (Fig. 3).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

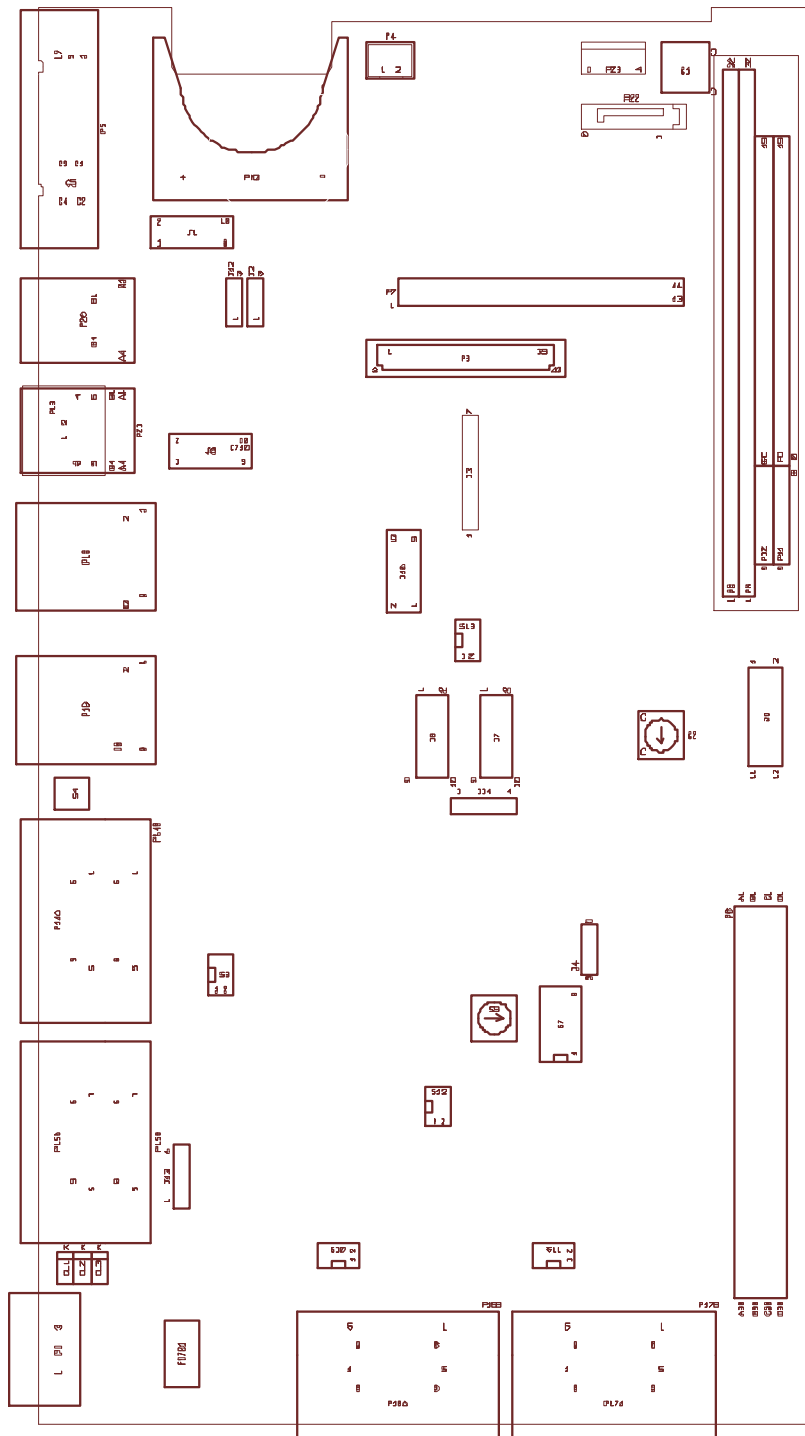


Fig. 2 Board Layout (IPC/NETSBC-7X)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The IPC/NETSBC-7A uses the same memory layout as a standard desktop PC. Onboard devices, DRAM, graphics controller and Boot Block Flash make use of the 4 GByte addressable memory space. Table 1 shows a typical configuration of the IPC/COMPACT7M1-1A with 1GB DRAM.

Address		Size	Device / Register	Remarks
0'0000'0000h	· 0009'FFFFh	640K	Main Memory (DRAM)	
0'000A'0000h	· 000B'FFFFh	128K	VGA Video Memory	
0'000C'0000h	· 000C'FFFFh	64K	Graphics BIOS	see paragraph 3.8.1 and 4.2.3
0'000D'0000h	· 000D'FFFFh	64K	PCI Bus	
0'000E'0000h	· 000F'FFFFh	128K	System BIOS	
0'0010'0000	· 03F4F'FFFFh	1012M	Main Memory (DRAM)	free Memory above 1M
0'3F50'0000	· 03FFF'FFFFh		8MB Graphic Memory (UMA) 3MB System	do not access
0'FFF0'0000	· FFFF'FFFFh	1024K	BIOS/BIOS Extensions	do not access

Tab. 1 Physical Memory Address Space Layout for IPC/COMPACT7M1-1A

Important Note

The main memory above 1M isn't fully usable for applications. The main memory for applications is shared with the graphics memory (UMA: Unified Memory Architecture). The graphics memory can be either configured to 4MB or 8MB. The default value is 8MB. BIOS and other System devices use memory above 1MB. Depending on enabled or disabled functions in the BIOS the amount of additional memory used can vary.

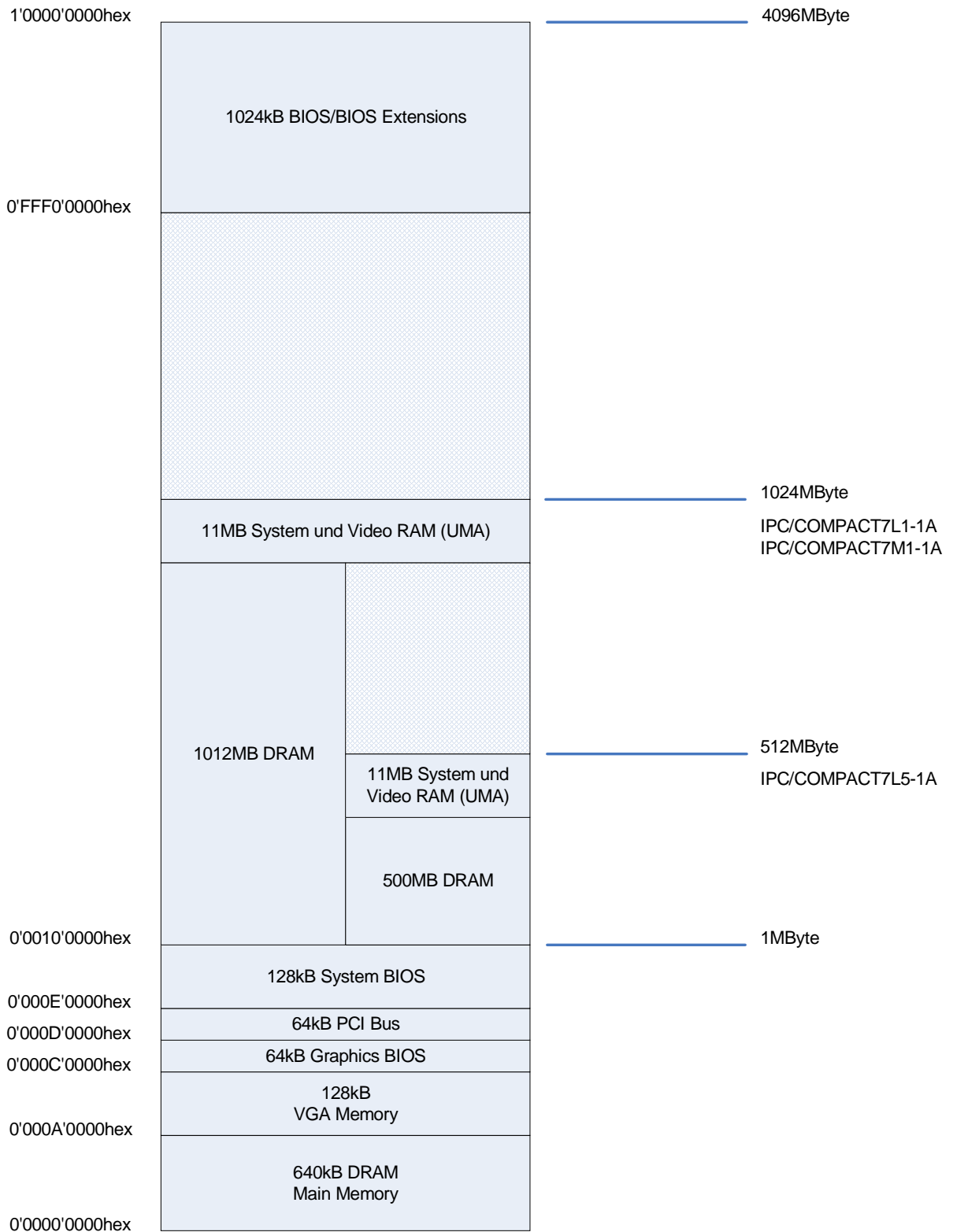


Fig. 3 Memory Map

3.2.2. General I/O Layout and Configuration

The IPC/NETSB's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Size	Device / Register	Remarks
0000h · 000Fh	16 Bytes	Slave DMA (8237)	
0020h · 0021h	2 Bytes	PIC master (8259)	command/status
0040h · 0043h	4 Bytes	PIT (8254)	
0060h ·	1 Byte	Keyboard/mouse	data port
0061h ·	1 Byte	Port B	control
0064h	1 Byte	keyboard/mouse	command/status
0070h · 0071h	2 Bytes	RTC RAM	address/data port
0072h · 0073h	2 Bytes	high RTC RAM	address/data port
0080h	1 Byte	POST code	
0081h · 0083h	2 Bytes	DMA low page	
0087h	1 Byte	DMA low page	
0092h	1 Byte	Port A	
00A0h · 00A1	2 Bytes	PIC slave (8259)	Command/Status
00C0h	1 Byte	master DMA	
00C2h	1 Byte	master DMA	
00C4			
0200h · 023F		free	avail. on PC/104 bus
0278 · 027Fh	16 Bytes	reserved for LPT2	
02E0 · 02EFh	16 Bytes	free	avail. on PC/104 bus
02F8 · 02FFh	8 Bytes	COM2	
0300h · 036Fh		free	avail. on PC/104 bus
0370h · 0372h	3 Bytes	reserved for Floppy 2	
0374h · 0375h	2 Bytes	reserved for Floppy 2	
0377h	1 Bytes	reserved for Floppy 2	
0378h · 037Fh	8 Bytes	reserved for LPT2	
03B0h · 03BBh	11 Bytes	VGA adapter	
03BCh · 03BFh	4 Bytes	reserved for LPT3	
03C0h · 03CFh	8 Bytes	VGA adapter	EGA
03D0h · 03DFh	8 Bytes	VGA adapter	CGA
03E0h · 03EFh	16 Bytes	free	avail. on PC/104 bus
03F0h · 03F2h	3 Bytes	reserved for Floppy 1	
03F4h · 03F5h	2 Bytes	reserved for Floppy 1	
03F6h	1 Byte	primary IDE channel	
03F7h	1 Byte	reserved for Floppy 1	

03F8h	· 03FFh	8 Bytes	COM1	
0481h	· 0483h	2 Bytes	DMA high page	
0487h		1 Bytes	DMA high page	
0489h	· 048Bh	3 Bytes	DMA high page	
048Fh		1 Byte	DMA high page	
04D0h	· 04D1h	2 Bytes	PIC	Level/Edge
0500h	· 07FFh	2048 Bytes	runtime registers SIO	Refer to Datasheet
0A78h		1 Byte	PnP	Configuration port
0CF8h	· 0CFFh	8 Bytes	PCI	Configuration register
2000h	· 2FFF	4096 Bytes	PCI-PCI bridge	
3000h	· 3FFFh	4096 Bytes	PCI-PCI bridge	
4000h	· 401Eh	29 Bytes	USB controller	
4020h	· 403Eh	29 Bytes	USB controller	
4040h	· 405EH	29 Bytes	USB controller	
4060h	· 406Eh	15 Bytes	IDE controller	
4070h	· 4076h	7 Bytes	VGA controller	
7600h	· 76FFh	256 Bytes	Free	avail. on PC/104 bus
7700h	· 77FFh	256 Bytes	Free	avail. on PC/104 bus
8200h	· 821Fh	16 Bytes	NETSBC-7 system register	
8220h	· 827Fh	128 Bytes	free	avail. on PC/104 bus
0'D000h	· 0'EFFh	1024 Bytes	Reserved for PCI device	VGA, LAN, USB, IDE

Tab. 2 I/O Address Space Layout

Only the I/O addresses which are marked with “avail. On PC/104 bus” can be accessed on the aforementioned connector and be used for additional peripherals. The other unused I/O space can't be accessed because these cycles are claimed by the integrated South Bridge and not by the PCI/ISA Bridge.

3.3. Intel Atom Z5xx Processor

The Intel Atom Z5xx Processor Family (Codename Silverthorne) is a highly integrated x86 processor for embedded applications.

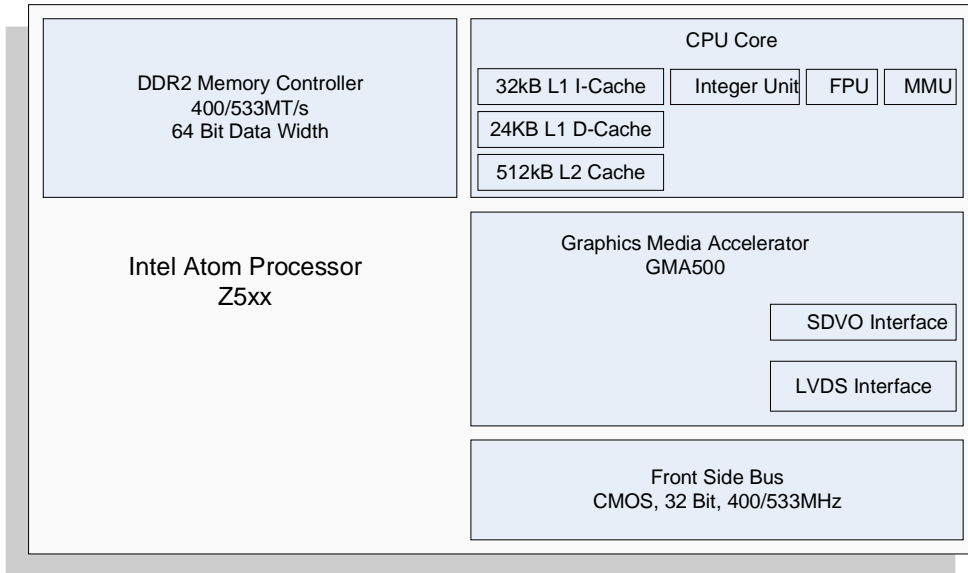


Fig. 4 Intel Atom Processor Z5xx

3.4. Intel System Controller Hub US15W

The Intel System Controller Hub US15 companion device is designed to work with the Atom Z5xx microprocessor.

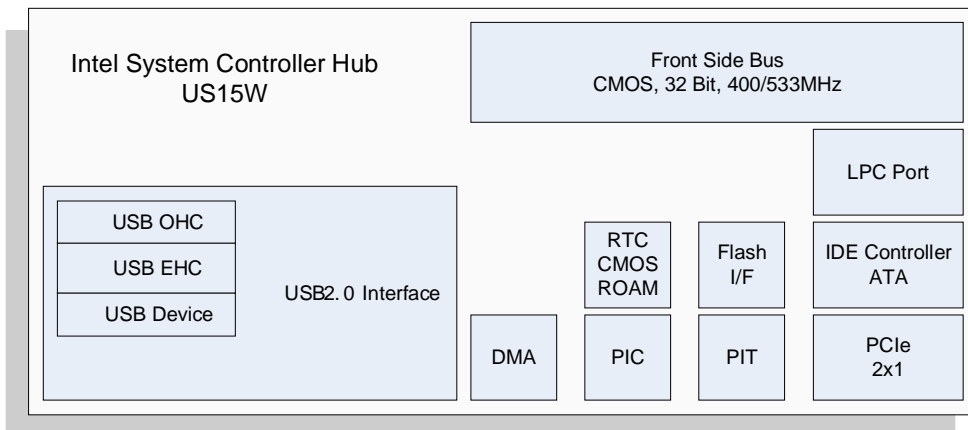


Fig. 5 Intel System Controller Hub US15W

3.5. PCI/PCIe Devices

All devices follow the PCI 2.2 and PCIe 1.0a specification. The BIOS (and/or OS) controls memory and I/O resources.

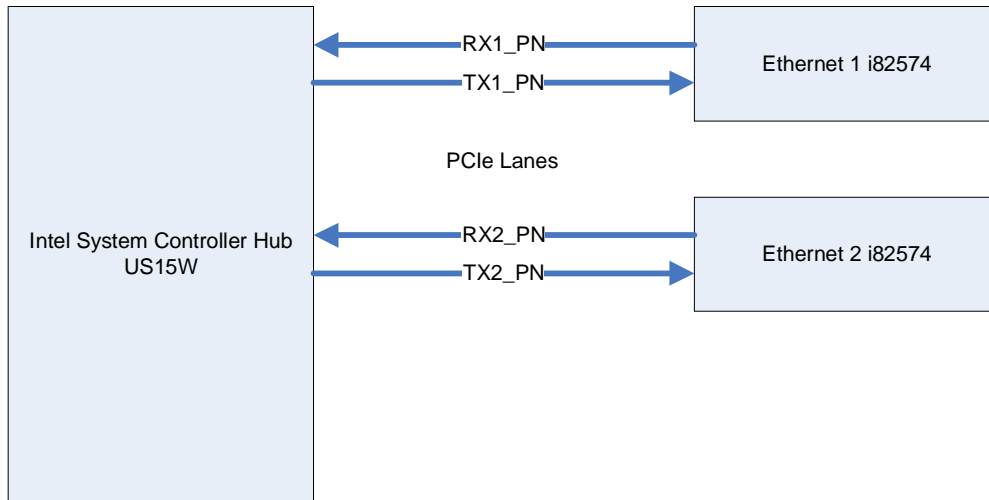


Fig. 6 PCI Express System

PCI Device	Vendor ID	Device ID	Bus/ Device/ Function	Interrupt INTline/ INTpin	Comment
Host Bridge	8086	8100	00/00/00		
Graphic Controller	8086	8108	00/02/00	0B/01	
PCI/PCI Bridge	8086	8110	00/1C/00	0B/01	
PCI/PCI Bridge	8086	8112	00/1C/01	0A/02	
USB Controller	8086	8114	00/1D/00	0B/01	
USB Controller	8086	8115	00/1D/01	0A/02	
USB Controller	8086	8116	00/1D/02	09/03	
System Peripheral	8086	811C	00/1E/00	0B/01	
System Peripheral	8086	811D	00/1E/01	0A/02	
System Peripheral	8086	811E	00/1E/02	09/03	
PCI/ISA Bridge	8086	8119	00/1F/00		
IDE Controller	8086	811A	00/1F/01	FF/00	
Ethernet Controller 1	8086	10D3	01/00/00	0B/01	ETH2
Ethernet Controller 2	8086	10D3	02/00/00	0A/01	ETH1

Tab. 3 PCI Devices

3.6. Hardware Interrupts

The Intel Atom processor Z5xx chipset integrates two legacy 8259-compatible Programmable Interrupt Controllers (PIC). The registers of the PIC can be accessed through the I/O ports 020h and 021h resp. 0A0h and 0A1h.

Device	IRQ	PCI IRQ	Comment
8254 Timer	0	-	Legacy
Keyboard	1	-	Legacy
8259	2	-	Slave controller
UART	3	-	COM2
UART	4	-	COM1
Free	5	-	Available on PC/104 bus
Free	6	-	Available on PC/104 bus
USB	7		
RTC	8	-	Legacy
Free	9	-	
PCI-PCI Bridge	10	-	
VGA Adapter	11	-	Do not use with other devices
Mouse	12	-	Legacy
FPU	13	-	Legacy
IDE	14	-	Primary IDE channel
Free	15	-	Available on PC/104 bus

Tab. 4 Hardware Interrupt Table

3.7. DMA Channels

DMA	Data Width	System Resource
0	8 bits	Available
1	8 bits	Available
2	8 bits	Available
3	8 bits	Available
4		Reserved, cascaded with channel
5	16 bits	IDE Controller
6	16 bits	Available
7	16 bits	Available

Tab. 5 DMA channels

3.8. Peripheral Devices

3.8.1. Scope

The peripheral devices described in this chapter are the core features of the IPC/NETSBC-7A board. Meaning that they're available on all the derivatives. Special features implemented only on one special board are described in a separate chapter of this documentation.

3.8.2. DVI Interface

The DVI (Digital Visual Interface) signals are available on the High Density DVI-D connector P5 for direct connection of DVI compatible monitors. The signals from the SDVO (Serial Digital Video Out) port are converted into DVI signals from the controller. The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).

Device Connection

Pin Number	Signal	Remarks
1	DATA#2	
2	DATA2	
3	Shield 2/4	Connected to GND
4	DATA#4	Not connected
5	DATA4	Not connected
6	DDC_CLK	
7	DDC_DATA	
8	NC	Not connected
9	DATA#1	
10	DATA1	
11	Shield 1/3	Connected to GND
12	DATA#3	Not connected
13	DATA3	Not connected
14	VCC5	+5Vdc
15	GND	
16	HPDET	Hot Plug Detect
17	DATA#0	
18	DATA0	
19	Shield 0/5	Connected to GND
20	DATA#5	
21	DATA5	
22	Shield CLK	Connected to GND
23	CLK	
24	CLK#	
C1	VGA_RED	Not connected
C2	VGA_GREEN	Not connected
C3	VGA_BLUE	Not connected
C4	HSYNC	Not connected
C5	VGA_GND	Not connected

Tab. 6 DVI-D connector P5

3.8.3. LVDS Interface

The Silverthorne processor has next to the SDVO a second graphic interface. The LVDS signals are on a internal header P3 available. The LVDS controller supports 18 and 24 bit color depth.

Device Connection

Pin Number	Signal	Remarks
1	V33	+3.3Vdc
2	V33	
3	GND	
4	GND	
5	V33	+3.3Vdc
6	V33	+3.3Vdc
7	GND	
8	GND	
9	DATA0N	
10	DATA0P	
11	DATA1N	
12	DATA1P	
13	DATA2N	
14	DATA2P	
15	CLKN	
16	CLKP	
17	DATA3N	
18	DATA3P	
19	GND	
20	GND	

21	NC	Not connected
22	NC	Not connected
23	NC	Not connected
24	NC	Not connected
25	ENAVCC	Power enable
26	BCK_ENA	Backlight enable
27	BKLT_CTRL	Backlight control
28	NC	Not connected
29	NC	Not connected
30	NC	Not connected
31	NC	Not connected
32	NC	Not connected
33	GND	
34	GND	
35	VCC	+5Vdc
36	VCC	+5Vdc
37	NC	Not connected
38	NC	Not connected
39	V33	+3.3Vdc
40	V33	+3.3Vdc

Tab. 7 LVDS header P3

3.8.4. VGA Interface

Instead of a SDVO/DVI converter a special SDVO/VGA (Video Graphics Array) converter can optionally be mounted. Please contact the manufacturer for MOQ and further information.

Device Connection

Pin Number	Signal	Remarks
1	VGA_RED	
2	VGA_GREEN	
3	VGA_BLUE	
4	GND	
5	NC	Not connected
6	GND	
7	HSYNC	
8	VSYNC	
9	DDC_DATA	
10	DDC_CLK	

Tab. 8 VGA header J1

On the standard board version no signals are connected to J1.

Important Note

Be careful when using the VGA or video signals on expansion boards. Special design and layout precautions must be met for these high speed analog signals.
Maximum cable length allowed for VGA connection is 15 m.
Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

3.8.5. IDE/CompactFlash-Interface

The IDE interface is setup as Primary IDE Channel with standard PC address decoding and using hardware interrupt 14. It supports 2 external devices on a single connection, one configured as master the other as slave. Alternatively one external device may be replaced by an on board pluggable CompactFlash card. The IDE timing is setup by software (BIOS autodetection).

The IDE interface provides the following configuration options:

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 2-4 open = on board CompactFlash is slave Pin 2-4 closed = on board CompactFlash is master	don't care if only external devices are connected.

Tab. 9 IDE Configuration Options

Device Connection

External IDE devices are connected through the standard 2x20 pin header P7. A CompactFlash card may be directly plugged in the on board CompactFlash connector P8.

Pin Number	Signal	Pin Number	Signal
1	RST#	2	GND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20	NC
21	DRQ	22	GND
23	HLOW#	24	GND
25	HIOR#	26	GND
27	IOCHRDY	28	GND
29	DACK#	30	GND
31	IRQ	32	NC
33	HA1	34	PDIAG#
35	HA0	36	HA2
37	HCS0#	38	HCS1#
39	DASP#	40	GND
41	VCC	42	VCC
43	GND	44	NC

Tab. 10 IDE Connector P7 (2x22 pin)

Important Notes

Do not connect 2 external devices and a CompactFlash card together. This may damage the system and the IDE devices.

Note

The IPC/NETSBC-7A offers a 5V supply (not fused) for direct plugin IDE/CompactFlash adapters. Max. allowed current drawing is 100mA.

3.8.6. Serial Ports 1/2

Two serial ports are available. The serial ports have fixed base addresses of 3F8H for COM1 and 2F8H for COM2. COM1 uses hardware interrupt 4 and COM2 uses hardware interrupt 3.

Device Connection

The Serial Port COM1 is available on the DSUB9 connector P14A (bottom).

The Serial Port COM2 is available on the DSUB9 connector P15A (bottom).

Pin Number	Signal	Remarks
1	DCD*	
2	RXD	
3	TXD	
4	DTR*	
5	GND	
6	DSR*	
7	RTS*	
8	CTS*	
9	RI*	

Tab. 11 Serial Ports COM1 and COM2

Optional RS485 Interface on COM2 Port

Important Note

This chapter will be added in a future release.

3.8.7. USB Interface

The IPC/NETSBC-7A features an OHCI/EHCI compatible USB Hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS. Four channels are available. USB2 can be configured as a USB device.

Device Connection

The USB interface uses two dual USB connectors.

P20 (top) Pin Number	USB channel 0 Signal	P20 (bottom) Pin Number	USB channel 1 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 12 Keyboard/Mouse internal Header J6 (2x5 pin)

P21 (top) Pin Number	USB channel 2 Signal	P21 (bottom) Pin Number	USB channel 3 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 13 Keyboard/Mouse internal Header J6 (2x5 pin)

3.8.8. PS/2 Keyboard/Mouse Interface

The keyboard signals are only available on an internal header J6. However a MiniDIN (PS/2 connector) can be mounted optionally instead of P21 (USB channels 2 and 3). The controller uses hardware interrupt 1 for the keyboard and hardware interrupt 12 for the mouse. The following configuration options are provided:

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 1-3, 2-4 closed = Keyboard signals on P13 Pin 3-5, 4-6 closed = Mouse signals on P13	Only if P13 is mounted

Tab. 14 Keyboard/Mouse Configuration Options

Device Connection

The standard PS/2 connector P13 is not mounted by default. The PS/2 signals are available on the internal header J6 (2x5 pin). P13 is used (if available) for direct connection of the keyboard or mouse (depending on jumper configuration).

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	P3-2	8	P3-6
9	GND	10	+5V (not fused)

Tab. 15 Keyboard/Mouse internal Header J6 (2x5 pin)

Important Note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
 Use shielded cables for maximum EMI protection.

3.8.9. Ethernet Interfaces

The IPC/NETSBC-7A features two PCIe Gigabit-Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. There are two LED's (yellow and green) integrated into the RJ45 connector. The green LED indicates speed. The LED will be on at 100Mbps and off at 10Mbps. The yellow“ activity” LED indicates either transmit or receive activity. When activity is present, the LED is on; when no activity is present, the LED is off.

No configuration options are available for the ethernet device.

Device Connection

The Ethernet interface uses the standard RJ45 connector P18 and P19 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 16 Ethernet Twisted Pair Interface Connector P18 and P19 (RJ45)

3.8.10. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the IPC/NETSBC-7A's hardware reset.

Configuration Options

Jumper	Configuration	Remarks
J6	Pin 4-6 open = 1.6 s Pin 4-6 closed = 100 ms	

Tab. 17 Watchdog Configuration Options

3.8.11. Power Supervision

This function is not implemented yet. Please contact manufacturer for further information.

Power Fail

This function is not implemented yet. Please contact manufacturer for further information.

Remote On/Off

This function is not implemented yet. Please contact manufacturer for further information.

3.8.12. Configurations Switches

There are two rotary Hex-Switches for customer use available, where only S1 can be accessed by removing the left side cover. The values can be read from a register at I/O address 820Ch. The higher nibble contains the value of S2, the lower nibble the value of S1.

3.8.13. Factory Programming Header

The programmable logic devices on the IPC/NETSBC-7A board are factory programmed using some pins of the internal header J5. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK	do not use
3	TDO	do not use
5	TMS	do not use
7	TDI	do not use

Tab. 18 Factory Programming Header J5 (2x5 pin)

3.8.14. LPC Header

The internal LPC (Low Pin Count) bus is available on the header J3. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	AD0	do not use
2	AD1	do not use
3	AD2	do not use
4	AD3	do not use
5	FRAME#	do not use
6	RST#	do not use
7	CLK	do not use

Tab. 19 LPC J3 (1x7 pin)

3.8.15. Isolated Power Supply

Instead of the synchronous buck controller a DC/DC converter can be soldered onto the board for isolating the power supply. The input range will be reduced. For further information please contact the manufacturer

3.9. Optional Functions

There are several functions in the IPC/COMPACT7-SL (on the IPC/NETSBC-7A board) which aren't implemented on the standard Syslogic product:

- isolated power supply
- GoldCap for battery backup of time/date of RTC
- RS485 interface at COM2
- up to two isolated CAN interfaces

For further technical information and customization details please contact Syslogic sales.

3.10. Hardware Limitations

There are no hardware limitations.

4 Programming Information

4.1. Overview

The programming of the IPC/NETSBC-7A board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

Please refer to chapter 3.6 for the table showing the usage of the IPC/NETSBC-7A's interrupts.

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming processor internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the IPC/NETSBC-7A system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 0.

Address	Device / Register	Remarks
8200h	Status Register	
8201h	Control Register	Reset state = 05H
8202h	Function ID Register	
8203h	reserved	do not write
8204h	Option ID Register	
8205h	Setup Register	Reset state = 00H
8206h	Revision ID Register	
8207h	reserved:	reserved, always write 0
8208h	reserved:	reserved, always write 0
8209h	reserved:	reserved, always write 0
820Ah	reserved:	reserved, always write 0
820Bh	I2C Register	for Temp Sensor
820Ch	Switch Register	do not write
820Dh	reserved	do not access
820F..821Fh	reserved	do not access

Tab. 20 IPC/NETSBC-7A System Registers

Status Register

Reading I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
OVERTMP*	LOBAT*	1	WDG*	1*	1	ERRINT*	reserved

Description:

- reserved: reserved for future use
- IOCHCHK*: Error Interrupt Status from ISA Bus
 0 = Error Interrupt pending on this module
 1 = no Error Interrupt pending on this module
- WDG*: Watchdog Status Flag
 0 = Watchdog has timed out
 1 = Watchdog running or disabled
 Reset by issuing a hardware reset (see register 8204H)
- LOBAT*: Battery Status Flag
 0 = Battery voltage low
 1 = Battery voltage ok
- OVERTMP*: Temperatur Sensor Status Flag
 0 = programmed temperatur limit reached
 1 = temperatur ok (below limit)

Writing I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Control Register

Reading I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
1	WDTRIG	WDNMI	STOP	1	1	0	1

Description:

- STOP: NETIPC STOP* Signal State
 0 = STOP* inactive (high)
 1 = STOP* active (low)
- WDNMI: Watchdog action Select
 0 = Watchdog timeout activates hardware reset
 1 = not supported
- WDTRIG: Watchdog Trigger
 any state change triggers the watchdog (timeout reset)

Writing I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	WDTRIG	reserved	STOP	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- STOP: NETIPC STOP* Signal State
 0 = STOP* inactive (high)
 1 = STOP* active (low)
- WDNMI: Watchdog action Select
 always write 0
- WDTRIG: Watchdog Trigger
 any state change triggers the watchdog (timeout reset)

Function ID Register

Reading I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
 0101'0001 (51h) = general NETIPC board,
 subtype defined by Option ID Register

Writing I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Option ID Register

Reading I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
OPT7	OPT6	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0

Description:

- OPT7..0: Option ID
 1100'0000 (C0h) = IPC/NETSBC-7x

Writing I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Description:

- xxxxxxxx: Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

Setup Register

Reading I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	0	0	0	0	0	0

Description:

- WDEN: Watchdog Enable
 0 = Watchdog disabled
 1 = Watchdog enabled (running)
- READY: NETIPC READY Signal State
 0 = READY inactive
 1 = READY active

Writing I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- WDEN: Watchdog Enable
 0 = Watchdog disabled (cannot be disabled while running)
 1 = enable Watchdog
- READY: NETIPC READY Signal State
 0 = deactivate READY
 1 = activate READY

Revision ID Register

Reading I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

- RID7..0: Revision ID
 xxH = Logic Design revision ID (see Tab. 31)

Writing I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

I2C Register (for temperature sensor control)

Reading I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	SCL	SDA	1	1	1	1

Description:

- SDA: Data Port Pin State
 0 = Pin State = Low
 1 = Pin State = High
- SCL: Clock Port Pin State
 0 = Pin State = Low
 1 = Pin State = High
- SDAO: Data Port Output Latch State
 0 = Output Latch State = Low
 1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output State
 0 = Output Latch State = Low
 1 = Output Latch State = High (Open Collector)

Writing I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	X	X	X	X	X	X

Description:

- SDAO: Data Port Output Latch
 0 = Output Latch State = Low
 1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output
 0 = Output Latch State = Low
 1 = Output Latch State = High (Open Collector)

Switch Register

Reading I/O Register 820Ch:

D7	D6	D5	D4	D3	D2	D1	D0
S2_3	S2_2	S2_1	S2_0	S1_3	S1_2	S1_1	S1_0

Description:

- S2_3: Data 2^3
- S2_2: Data 2^2
- S2_1: Data 2^1
- S2_0: Data 2^0

- S1_3: Data 2^3
- S1_2: Data 2^2
- S1_1: Data 2^1
- S1_0: Data 2^0

Writing I/O Register 820Ch:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	Reserved

Description:

reserved: reserved, do not write

4.3. Peripheral Devices

4.3.1. VGA-Interface

The VGA interface uses the standard PC/AT VGA register set. For detailed programming information please refer to the IBM PC/AT Technical Reference or similar documentation.

Low level programming is handled by the VESA compatible VGA-BIOS.

4.3.2. IDE-Interface

The IDE interface uses the standard PC/AT register set. For detailed programming information please refer to the IBM PC/AT Technical Reference, ATA/ATAPI standards (ANSI) or similar documentation.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit FIFOs. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation. I/O base addresses and IRQ can be modified through BIOS.

4.3.4. Keyboard/Mouse Interface

The Keyboard/Mouse interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 82C42 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.5. Ethernet Interfaces

On the IPC/NETSBC-7x board the Ethernet interfaces use the Intel 82574 Gigabit Ethernet Controller. For detailed programming information and drivers check www.syslogic.com or www.intel.com.

4.3.6. Temperature Sensor

The Temperature Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the NETSBC-6A. The LM75 can be accessed at the I2C address 00h. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.

Poweron default setting for OVERTMP* is 80°C chip temperature.

I2C Address	Device	Remarks
00h	LM75	

Tab. 21 I2C Address Space

4.3.7. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.

If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the Setup Register.

The watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the Control Register. The application must check the WDG* bit in the Status Register upon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.

For sample code please contact Syslogic.

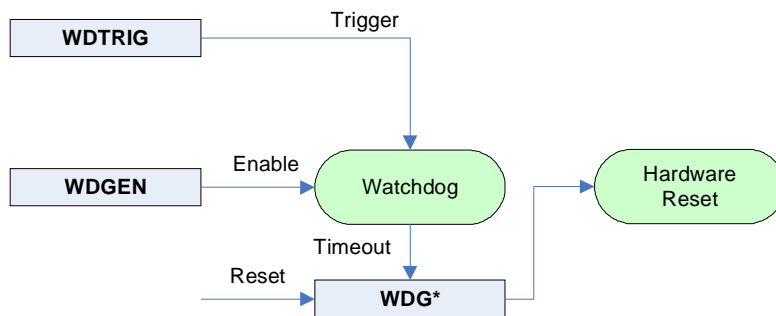


Fig. 7 Watchdog Blockdiagram

The watchdog can only initiate a hardware reset. The NMI option is not supported.

5 Enclosure, Assembly and Mounting

5.1. IPC/COMPACT7-SL Dimensions

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see paragraph 1.5).



Fig. 8 IPC/COMPACT7MI-1A

Important Notes

Before assembling the whole enclosure with the electronic modules please read through the following paragraphs containing information about the assembling of the system.

5.2. Internal Cabling

No internal cabling has to be done.

5.3. Serviceable Parts

The IPC/COMPACT7-SL contains two removable parts inside:

- Backup-Battery
- CompactFlash card (has to be ordered separately)

In order to exchange these parts, you must remove the cover by executing steps 1 and 2 of the following instructions.

Important Notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.

Important Notes

- The battery socket is coded, no wrong insertion of the backup battery is possible.
- Handle the flash memory module with care. In order to simplify the removal of the memory module a small commercially available tape can be applied to the compact flash which allows an easy grab of the module.

1. Remove 4 torx screws (M2x5, BN3803) on the side of the case.
2. Remove the side cover.
3. Exchange the battery or the Compact Flash card.

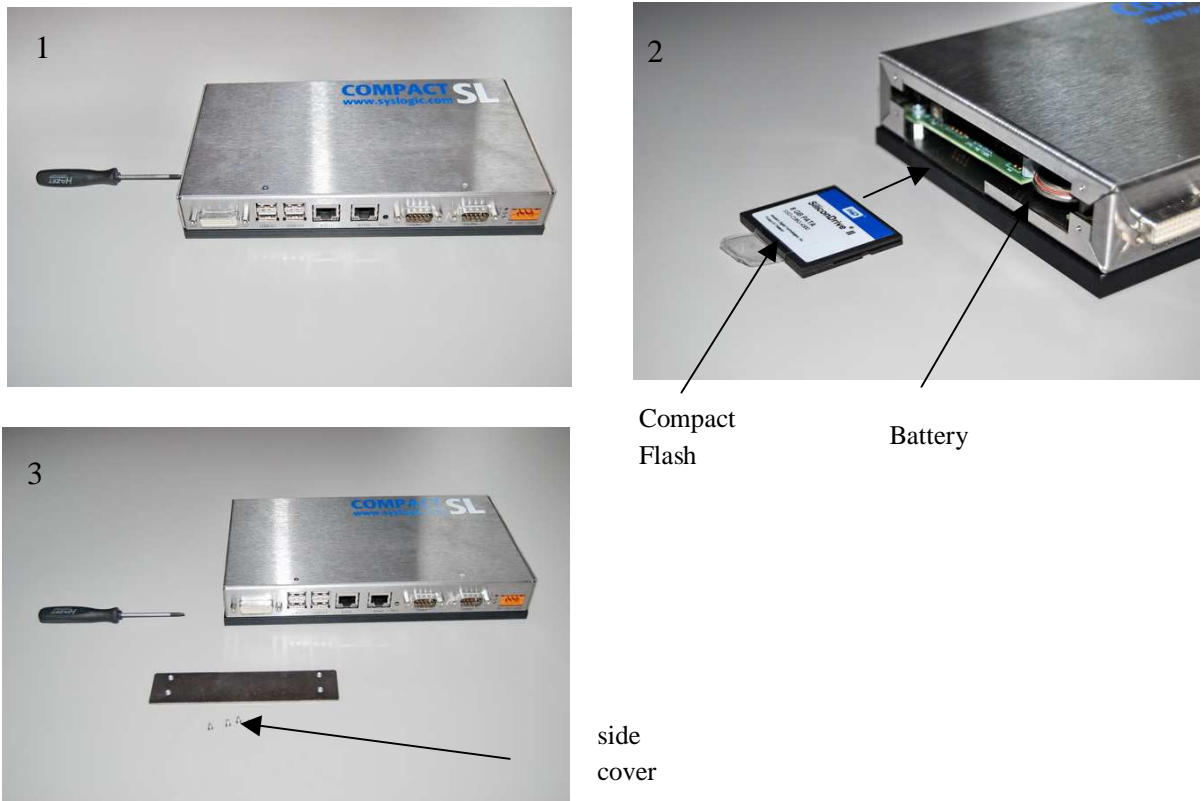


Fig. 9 Service of battery or Compact Flash card

5.4. Final Mounting of the Enclosure

As mentioned in chapter 1.4.1 there are additional mounting kits which have to be ordered separately. The mounting kits help to install the IPC/COMPACT7-SL into your electric control cabinet.

Important Notes

Be sure to use the correct screws; screws which are too long can damage the boards inside of the enclosure.

5.4.1. Rear Mounting

Product order code: IPC/MKITCP-1A

Document order code: DOC/IPC_MKITCP-1AE



Fig. 10 Rear mounting of the IPC/COMPACT7-SL (product image may vary)

5.4.2. Vertical Bottom Mounting

Product order code: IPC/MKITCP-2A

Document order code: DOC/IPC_MKITCP-2AE



Fig. 11 Vertical bottom mounting of the IPC/COMPACT7-SL (product image may vary)

5.4.3. Horizontal Bottom mounting

Product order code: IPC/MKITCP-2C

Document order code: DOC/IPC_MKITCP-2CE



Fig. 12 Horizontal bottom mounting of the IPC/COMPACT7-SL (product image may vary)

5.4.4. DIN Rail Mounting

Product order code: IPC/MKITCP-2E

Document order code: DOC/IPC_MKITCP-2EE



Fig. 13 One possible way of mounting the IPC/COMPACT6-SL onto the DIN-Rail

6 Installation and Cabling

6.1. Introduction

Installation and cabling of the IPC/COMPACT7-SL system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail or mounting kit.

Important Note

Before applying power to the IPC/COMPACT7-SL system, the NETSBC-7A board must be configured correctly and mounted.

Important Notes

To meet the requirements of RFI "CE"-certification, correct mounting, installation and cabling of the IPC/COMPACT7-SL system according to these guidelines is absolutely necessary.

6.2. Powering the IPC/COMPACT7-SL System

The "logic voltage", i.e. the power driving the electronic circuits (CPU and base board) is applied from a 24VDC power supply (10VDC...30VDC). The internal power supply converts the input voltage to the logic voltage level. Remember that the power supply is unisolated. For an isolated version please contact the manufacturer. The input voltage is applied with a 3pin Weidmüller connector:

Pin	Description
GND (1)	Ground
VDC (2)	VDC
PF (3)	Not used, do not connect

Tab. 22 Power connector pinout

The connector can be ordered directly at your Weidmüller distributor (order code: *BL3.5/3F*).

Order Code	Type
1606650000	BL3.5/3F

Tab. 23 Weidmüller power connector

When selecting the 24VDC power supply the maximum power dissipation of the system has to be considered.

Important Notes

Please make sure that the input voltage does not exceed 30V otherwise the base board could get damaged. If the input voltage drops below 10V the system doesn't work properly, correct operation cannot be guaranteed. The best efficiency of the power supply can be achieved if the external input voltage is around 24V. Therefore the power loss of the power supply circuitry is at its minimum. When operating the system at high temperatures please make sure that the power supply is around 24V.

The power fail and external shutdown functions (pin 3) are only available on system with revision 2 or higher.

6.3. Cabling the Interfaces



Fig. 14 Front view with connector markings (product image may vary)

Connector Marking	Interface Type
DVI	CRT
USB0/1	USB0 (bottom) / USB1 (top)
USB2/3	USB2 (bottom) / USB3 (top)
ETH1	Ethernet 1 (PCI device 13)
ETH2	Ethernet 2 (PCI device 12)
RST	Reset button
COM1	COM1: RS232
COM2	COM2: RS232 (or RS485)
red LED	(B): Busy
yellow LED	(D): Disk
green LED	(R): Run
PF VDC GND	Power Supply

Tab. 24 IPC/COMPACT7M71-1A: Connectors

6.4. Grounding

In some cases it is recommended to connect the shields of the cables to chassis potential at the entry point into the housing cabinet as shown in Fig. 15. If the cables enter a hermetically closed cabinet, use special 360 degree metal clamps (RFI protected types which contact to the cable shield).

Important Notes

Grounding of the cables shields using "pig-tail wires" are not recommended because of their high impedance at high frequencies. It is better to clamp the shields onto a grounded copper rail.

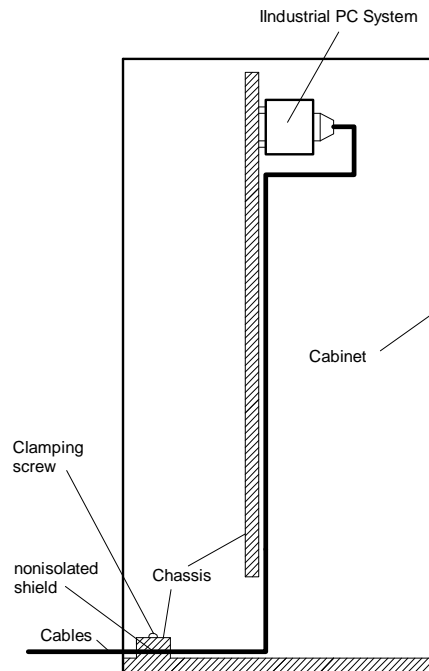


Fig. 15 Additional grounding of the cable shields at the entry point of a cabinet.

6.5. Cabling of Communication Links

If the communication ports are unisolated ports, cable shields have to be connected to chassis potential on both sides of the interconnection cable. If the cable is very long, a thick copper wire (10 mm²) for potential adjustment is highly recommended. Fig. 16 shows a non isolated system with common chassis ground.

Some of the communication ports are galvanically isolated ports (for more information please refer to the documentation of the base board and the CPU board): in such cases the shield of the interconnection cable must be wired to chassis potential only on one side of the cable. Fig. 17 shows an isolated system with independent grounds.

Important Notes

Grounding of cable shields using "pig-tails wires" are not recommended because of their high impedance at high frequencies. It is recommended to clamp the shields onto a grounded copper-rail.

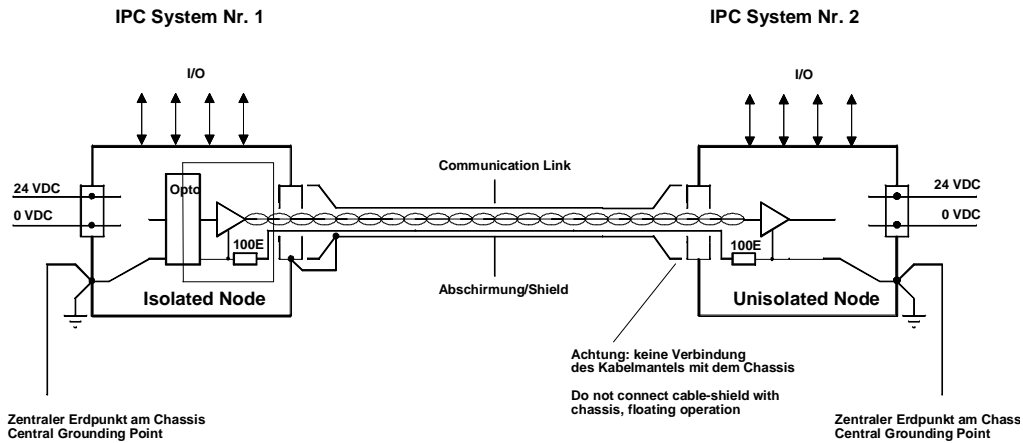


Fig. 16 Non isolated communication link with common chassis potential

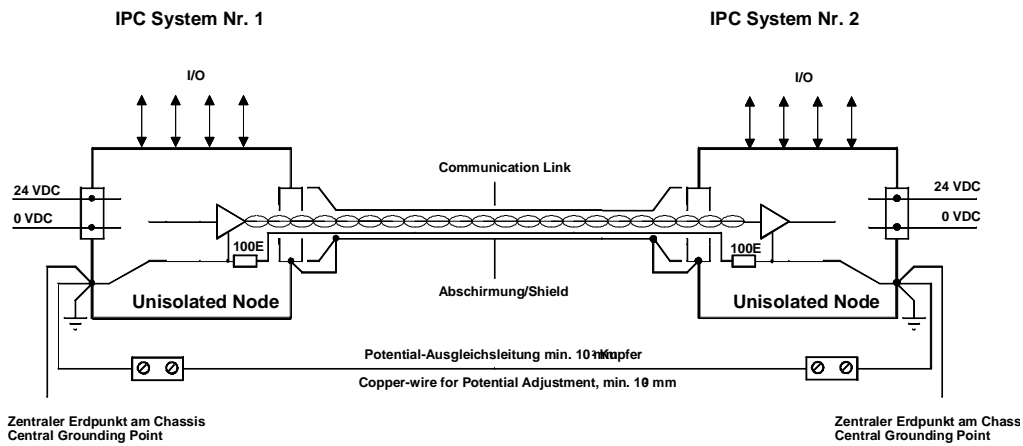


Fig. 17 Isolated communication link

7 Technical Data

7.1. Electrical Data

Important Note

Do not operate the IPC/COMPACT7-SL outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		1000			Vdc
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to PC/104 mounting holes		0.5			mm
RJ45 to logic		2.5			mm
RJ45 to chassis and PCB boarder		2.0			mm
storage temperature range	Tst	-40		90	°C

Tab. 25 General Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
external supply voltage	Vext	10.0	24.0	30.0	Vdc
battery backup voltage	Vbatt	2.70	3.00	3.60	Vdc
operating free-air temperature range (standard products)	Ta	0		55	°C

Tab. 26 General Recommended Operating Conditions

Electrical Characteristics (over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	Typ	max	Unit
IPC/COMPACT7L5-1A					
external supply current @ 10Vdc	Iext		0.70	0.80	A
full load power dissipation @ 10Vdc	Pmax		7.00	8.00	W
external supply current @ 24Vdc	Iext		0.33	0.37	A
full load power dissipation @ 24Vdc	Pmax		7.92	8.88	W
IPC/COMPACT7L1-1A					
external supply current @ 10Vdc	Iext		0.71	0.83	A
full load power dissipation @ 10Vdc	Pmax		7.10	8.30	W
external supply current @ 24Vdc	Iext		0.33	0.38	A
full load power dissipation @ 24Vdc	Pmax		7.92	9.12	W
IPC/COMPACT7M1-1A					
external supply current @ 10Vdc	Iext		0.78	1.00	A
full load power dissipation @ 10Vdc	Pmax		7.80	10.00	W
external supply current @ 24Vdc	Iext		0.36	0.45	A
full load power dissipation @ 24Vdc	Pmax		8.64	10.80	W
General specification					
Vbatt loading (Vcc=5V)	Ibat(on)		3	6.0	uA
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			2		V

Tab. 27 General Electrical Characteristics

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
IPC/COMPACT7L5-1A					
processor clock	pclk			1.1	GHz
memory clock (DDR400)	mclk			200	MHz
memory transfer rate				400	MT/s
IPC/COMPACT7L1-1A					
processor clock	pclk			1.1	GHz
memory clock (DDR400)	mclk			200	MHz
memory transfer rate				400	MT/s
IPC/COMPACT7M1-1A					
processor clock	pclk			1.6	GHz
memory clock (DDR533)	mclk			267	MHz
memory transfer rate				533	MT/s
General specification					
COM1/2 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock 1	fclk1		14.318		MHz
Timer base clock 1 accuracy				+/-100	ppm
Timer base clock 2	fclk2		32.768		kHz
Timer base clock 2 accuracy				+/-20	ppm
Timer base clock 2 aging				+/-3	ppm/year
Real Time Clock base clock	fclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C) ²
Real Time Clock aging				+/-3	ppm/year

Tab. 28 General Switching Characteristics

7.2. EMI / EMC Specification

7.2.1. Relevant Standards

The IPC/NETIPC-6 has been designed to comply the the following standards:

- EN 55022 Information technology equipment-
Radio disturbance characteristics-
Limits and methods of measurement

- EN 55024 Information technology equipment-
Immunity characteristics -
Limits and methods of measurement

- EN 61000-6-2 Electromagnetic compatibility (EMC),
Part 6-2: Generic standards- Immunity for industrial
environments

- EN 61000-6-4 Electromagnetic compatibility (EMC),
Part 6-4: Generic standards – Emission standard for
industrial environments

7.2.2. Emission

The emission tests are still pending. For furhter information please contact the manufacturer.

Test	Limit	Performance Criteria	Result	Remarks
Stationary interference voltage on the AC voltage terminals V-Network 0.15 – 30 MHz Power supply line Control and singal lines	EN 55022	Class A	pending	Compliant with EN 50121-3-2 (referring to EN 55011)
Radiated E-Field, horizontal and vertical polarized E-Field-Anenna 30 – 100 MHz EUT with all cables	EN 55022	Class A	pending	Compliant with EN 50121-3-2 (referring to EN 55011)

Tab. 29 Electromagnetic Emission

7.2.3. Immunity

The immunity tests are pending. For further information please contact the manufacturer.

Test	Standard Test level	Performance Criteria	Result	Remarks
Electrostatic discharge (ESD) - indirect on coupling plane with contact discharge - direct on case with air and contact discharge EUT with all cables	EN 61000-4-2 6kV Cont. 8kV Air (metal case)	 B B	 pending pending	Compliant with EN 50121-3-2
Radiated electromagnetic field 80 – 1000 MHz, 80% AM (1kHz) EUT with all cables	EN 61000-4-3 20V/m	 A	 pending	Compliant with EN 50121-3-2
Radiated electromagnetic field 1.4 – 2.0 GHz, 80% AM (1kHz) 2.0 – 2.7 GHz, 80% AM (1kHz) EUT with connection cable	EN 50121-3-2 10V/m 5V/m	 A A	 pending pending	
Fast transients (EFT) Common Mode, 5/50ns, repetition freq. 5kHz Control and signal lines Power supply	EN 61000-4-4 2kV 2kV	 B B	 pending pending	Compliant with EN 50121-3-2
Slow transients (Surges) Pulse form 1.2/50us Power supply All other signal lines (L>30m)	EN 61000-4-5 2.0kV (ground) 1.0kV	 B	 pending	Compliant with EN 50121-3-2
Conducted radio frequency 150kHz – 80MHz, 1kHz 80% AM Control and signal lines (L > 3m) Power supply	EN 61000-4-6 10V 10V	 A A	 pending pending	Compliant with EN 50121-3-2

Tab. 30 Electromagnetic Immunity

7.3. Environmental Specification

The IPC/COMPACT7 has been designed to meet the the following standards:

- EN 60068-2-27 Basic environmental testing procedures – Part 2-27:
Test Ea and guidance: Shock
- EN 60068-2-6 Environmental testing – Part 2-6:
Test Fc: Vibration (sinusoidal)

7.4. Mechanical Data

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see chapter 7.2). If you need detailed information of the enclosure do not hesitate to contact the manufacturer. We can provide you with the technical drawings.

8 Firmware

8.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System

Note : Refer to the BIOS documentation for detailed information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs

Note : Refer to the OS documentation for detailed information

Application Programs

- Initialization of IPC/COMPACT7-SL system, communications and external devices
- Start procedure for the Control Tasks

Note : Refer to the Application Programs documentation for detailed information

8.2. Application Programming Interface (API)

The IPC/COMPACT7-SL (IPC/NETSBC-7A board) does not contain any special API besides the installed BIOS.

8.3. Operating Systems

Syslogic offers an implementation for the following operating systems (OS):



Debian Linux Distribution
IPC/DEBIAN-50A



Microsoft Windows CE6.0
IPC/WINCE-60A



Microsoft Windows Embedded
Standard 2009
IPC/WINESTD09-7A

Others on request.

Important Note

When implementing a BSP for a new OS be sure to use the "Pentium Platform".

9 Product Revision History

9.1. Hardware

This paragraph lists the different hardware revisions of the IPC/COMPACT7-SL with integrated IPC/NETSBC-7A board delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Logic Revision ID Register	Remarks
IPC/COMPACT7L5-1A	#1		Original Release, RoHS compliant
IPC/COMPACT7L1-1A	#1		Original Release, RoHS compliant
IPC/COMPACT7M1-1A	#1		Original Release, RoHS compliant
IPC/NETSBC-7A	#1	03h	Original Release, RoHS compliant

Tab. 31 Hardware Revision State

9.2. Firmware/BIOS

Board Identification (see product label)	BIOS Version	Remarks
IPC/COMPACT7L5-1A	00170701	Prototype Release
IPC/COMPACT7L1-1A	00170701	Prototype Release
IPC/COMPACT7M1-1A	00170701	Prototype Release
IPC/COMPACT7L5-1A	00170702	Original Release, C6 disabled
IPC/COMPACT7L1-1A	00170702	Original Release, C6 disabled
IPC/COMPACT7M1-1A	00170702	Original Release, C6 disabled

Tab. 32 BIOS Revision State

Important Note

This document always covers the latest product revision listed in Tab. 31.
 Please contact the manufacturers technical support for upgrade options.

10 Manufacturer Information

10.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Täferstrasse 28
CH-5405 Baden-Dättwil / Switzerland

Email: info@syslogic.ch
www: <http://www.syslogic.com>
Phone +41 (0)56 200 90 40
Fax: +41 (0)56 200 90 50

Technical support:
support@syslogic.ch